

# SN75446, SN75447 DUAL PERIPHERAL DRIVERS

SLRS020A – DECEMBER 1978 – REVISED NOVEMBER 1995

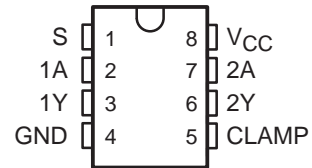
- Very Low Power Requirements
- Very Low Input Current
- Characterized for Use to 350 mA
- No Output Latch-Up at 50 V (After Conducting 300 mA)
- High-Voltage Outputs (70 V Min)
- Output Clamp Diodes for Transient Suppression (350 mA, 70 V)
- TTL- or MOS-Compatible Diode-Clamped Inputs
- Standard Supply Voltage
- Suitable for Hammer-Driver Applications

## description

The SN75446 and SN75447 dual peripheral drivers are designed for use in systems that require high current, high voltage, and fast switching times. The SN75446 and SN75447 provide AND and NAND drivers, respectively. These devices have diode-clamped inputs as well as high-current, high-voltage inductive-clamp diodes on the outputs.

The SN75446 and SN75447 drivers are characterized for operation from 0°C to 70°C.

## D OR P PACKAGE (TOP VIEW)



## Function Tables

SN75446  
(each AND driver)

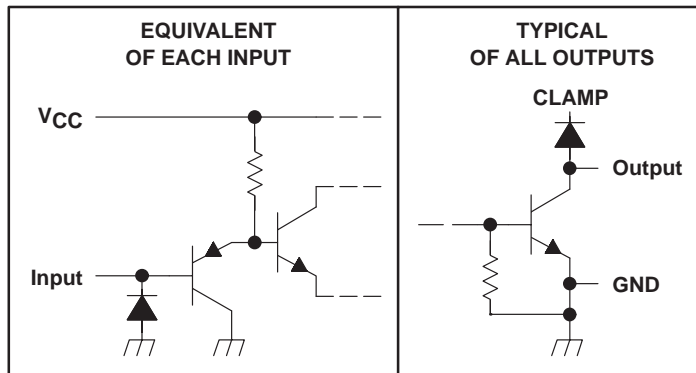
INPUTS		OUTPUT
A	S	Y
H	H	H
L	X	L
X	L	L

SN75447  
(each NAND driver)

INPUTS		OUTPUT
A	S	Y
H	H	L
L	X	H
X	L	H

H = high level, L = low level  
X = irrelevant

## schematics of inputs and outputs



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

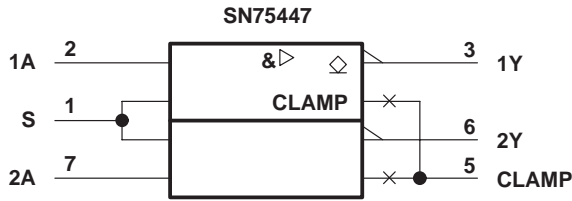
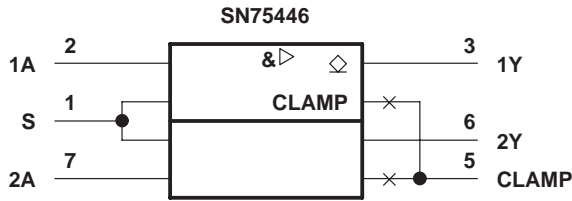
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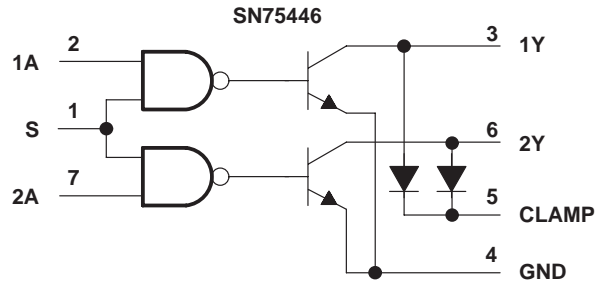
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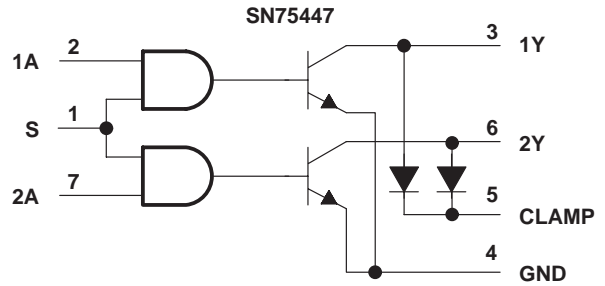
## logic symbols†



## logic diagrams (positive logic)



Positive Logic:  $Y = \overline{AS}$  or  $\overline{A+S}$



Positive Logic:  $Y = \overline{AS}$  or  $\overline{A+S}$

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC publication 617-12.

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage, $V_{CC}$ (see Note 1)	7 V
Input voltage, $V_I$	5.5 V
Output current, $I_O$ (see Note 2)	400 mA
Output clamp-diode current	400 mA
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, $T_A$	0°C to 70°C
Storage temperature range, $T_{stg}$	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. Voltage values are with respect to network GND.

2. Both halves of this dual circuit may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation ratings.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

## recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, $V_{CC}$	4.75	5	5.25	V
High-level input voltage, $V_{IH}$	2			V
Low-level input voltage, $V_{IL}$			0.8	V
Operating free-air temperature range, $T_A$	0		70	°C

## electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
$V_{IK}$	Input clamp voltage	$I_I = -12 \text{ mA}$		-0.9	-1.5		V
$V_{OL}$	Low-level output voltage	$V_{CC} = 4.75 \text{ V},$ $V_{IH} = 2 \text{ V},$ $V_{IL} = 0.8 \text{ V}$	$I_{OL} = 100 \text{ mA}$	0.1	0.3		V
			$I_{OL} = 200 \text{ mA}$	0.22	0.45		
			$I_{OL} = 300 \text{ mA}$	0.45	0.65		
			$I_{OL} = 350 \text{ mA}$	0.55	0.75		
$V_{O(BR)}$	Output breakdown voltage	$V_{CC} = 4.75 \text{ V},$	$I_{OH} = 100 \mu\text{A}$	70	100		V
$V_{R(K)}$	Output clamp-diode reverse voltage	$V_{CC} = 4.75 \text{ V},$	$I_R = 100 \mu\text{A}$	70	100		V
$V_{F(K)}$	Output clamp-diode forward voltage	$V_{CC} = 4.75 \text{ V},$	$I_F = 350 \text{ mA}$	0.6	1.2	1.6	V
$I_{OH}$	High-level output current	$V_{CC} = 4.75 \text{ V},$ $V_{IL} = 0.8 \text{ V},$	$V_{IH} = 2 \text{ V},$ $V_{OH} = 70 \text{ V}$		1	100	$\mu\text{A}$
$I_{IH}$	High-level input current	$V_{CC} = 5.25 \text{ V},$	$V_I = 5.25 \text{ V}$		0.01	10	$\mu\text{A}$
$I_{IL}$	Low-level input current	A input	$V_{CC} = 5.25 \text{ V},$ $V_I = 0.8 \text{ V}$		-0.5	-10	$\mu\text{A}$
		S input			-1	-20	
$I_{CCH}$	Supply current, outputs high	SN75446	$V_{CC} = 5.25 \text{ V}$	$V_I = 5 \text{ V}$	11	18	mA
		SN75447		$V_I = 0$	11	18	
$I_{CCL}$	Supply current, outputs low	SN75446	$V_{CC} = 5.25 \text{ V}$	$V_I = 0$	11	18	mA
		SN75447		$V_I = 5 \text{ V}$	11	18	

† All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ .

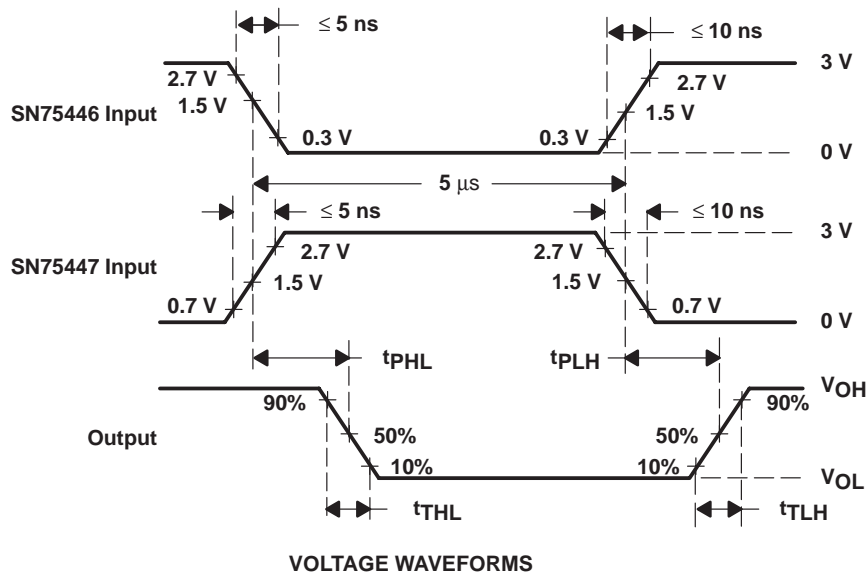
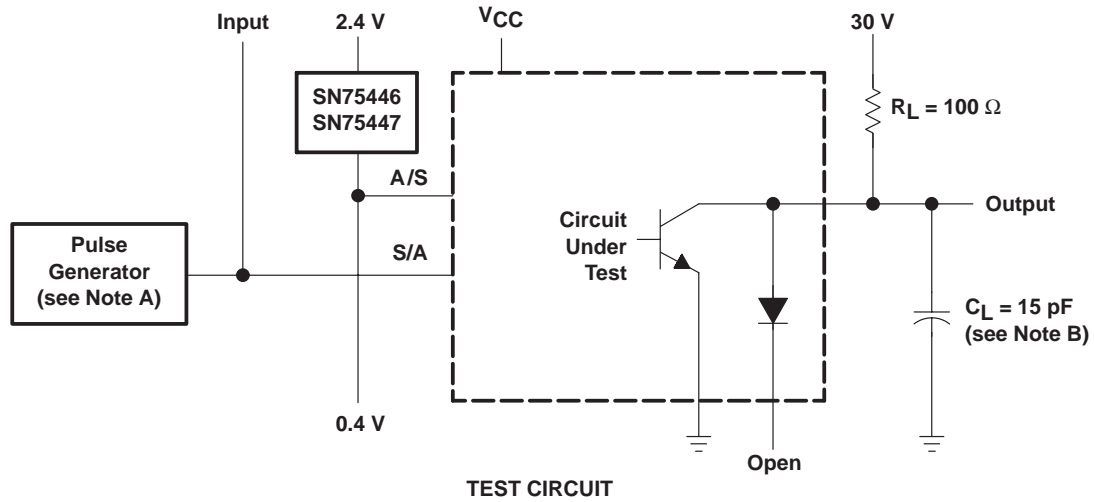
## switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{PLH}$	Propagation delay time, low-to-high-level output	$C_L = 15 \text{ pF},$ $R_L = 100 \Omega,$ See Figure 1			300	750	ns
$t_{PHL}$	Propagation delay time, high-to-low-level output				200	500	ns
$t_{TLH}$	Transition time, low-to-high-level output				50	100	ns
$t_{THL}$	Transition time, high-to-low-level output				50	100	ns
$V_{OH}$	High-level output voltage after switching	$V_S = 55 \text{ V},$ See Figure 2	$I_O \approx 300 \text{ mA},$	$V_S - 0.018$			V

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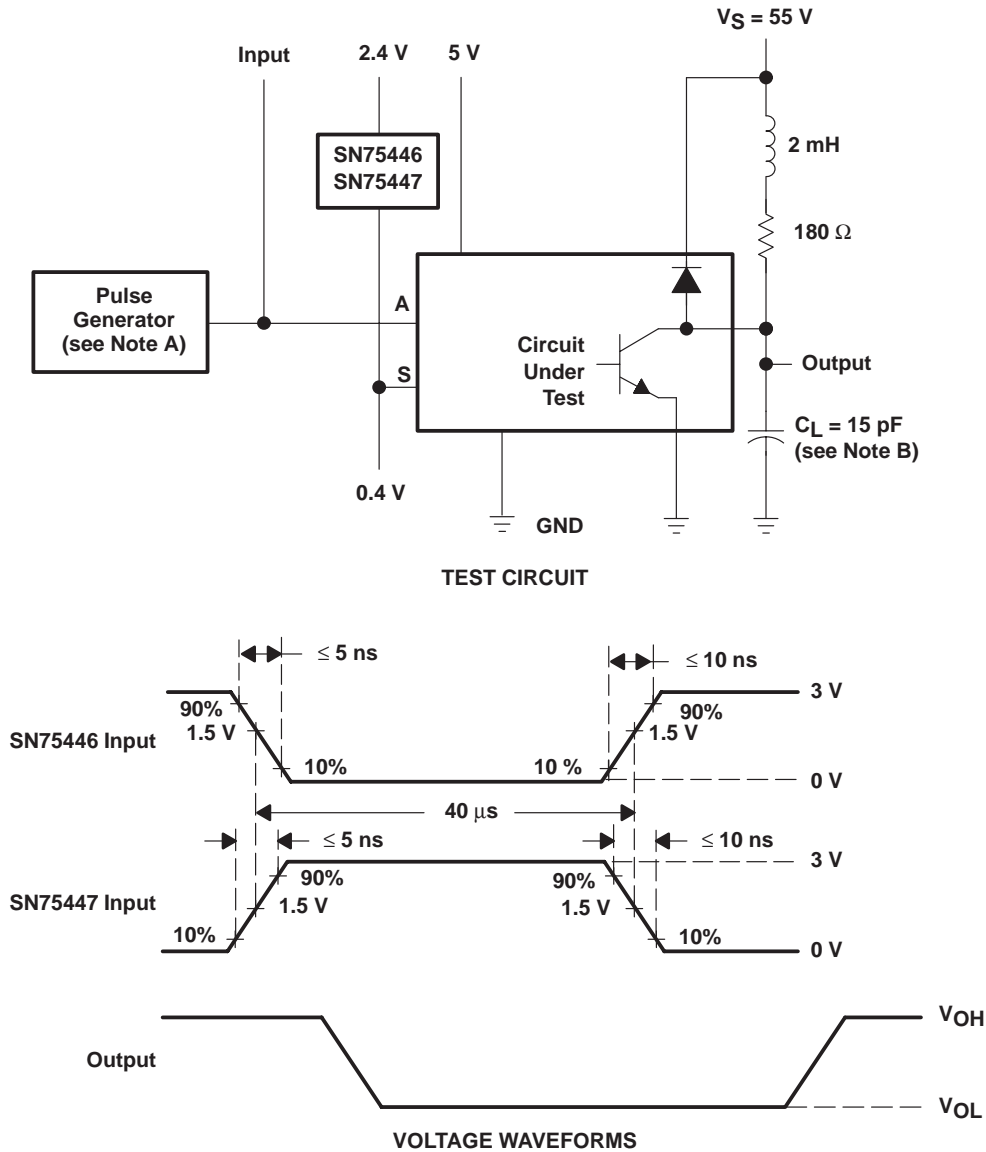
## PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The pulse generator has the following characteristics: PRR = 100 kHz,  $Z_O = 50 \Omega$ .  
B.  $C_L$  includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms, Switching Characteristics

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 kHz,  $Z_O = 50 \Omega$ .  
B.  $C_L$  includes probe and jig capacitance.

Figure 2. Latch-Up Test Circuit and Voltage Waveforms



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